

WHAT IS CLAIMED IS:

1. An extending circuit for memory which has an internal FIFO circuit and is connected with an external FIFO circuit, in order to extend memory capacity used for writing input data, comprising:

an output data effective signal generator which, when, based on a status signal output from said external FIFO circuit, judged that said external FIFO circuit can write data, makes said external FIFO circuit perform writing operation, for outputting said input data into said external FIFO circuit; and

an internal FIFO write enable generator which, when, based on said status signal output from said external FIFO circuit, judged that said external FIFO circuit can not write data, makes said internal FIFO circuit perform writing operation, for writing said input data into said internal FIFO circuit.

2. The extending circuit for memory according to claim 1, further comprising:

an internal FIFO read enable generator which, when, based on said status signal output from said external FIFO circuit and a status signal output from said internal FIFO circuit, judged that said external FIFO circuit can write data and said internal FIFO circuit is having memory data, makes said internal FIFO circuit perform reading operation, for read said memory data out from said internal FIFO circuit and outputting said memory data to said external FIFO circuit; and

an output data generator which, when said external FIFO circuit is judged being able to write data; and said internal FIFO circuit is judged having memory data; and said input data is received, outputs, prior to said input data, said memory data read out from said internal FIFO circuit to said

external FIFO circuit.

3. A transmitting-receiving device using the extending circuit for memory according to claim 2 for extending memory to be connected with either a transmission FIFO circuit or a reception FIFO circuit in a switching manner in order to extend a memory capacity, the transmitting-receiving device using extending circuit for memory using the Extending circuit for memory comprising:

a first selector for enabling either a transmission signal system or a reception signal system to be connected with the Extending circuit for memory in a switching manner;

a second selector for enabling a status signal from either the transmission FIFO circuit or the reception FIFO circuit to be connected with the internal FIFO write enable generator, the output data effective signal generator, and the internal FIFO read enable generator of the Extending circuit for memory in a switching manner;

a third selector for enabling the transmission FIFO circuit to be connected with either the output data generator and the output data effective signal generator of the Extending circuit for memory or the transmission signal system in a switching manner; and

a fourth selector for enabling the reception FIFO circuit to be connected with either the output data generator and the output data effective signal generator of the Extending circuit for memory or the reception signal system in a switching manner.

4. The transmitting-receiving device using extending circuit for memory using the Extending circuit for memory according to claim 3, further

comprising:

a control section for:

receiving status signals from the transmission FIFO circuit and the
reception FIFO circuit, when the transmission FIFO circuit is in a data
5 writable state and the reception FIFO circuit is in a data unwritable state,
connecting the first selector with the reception signal system and connecting
the second and the third selectors with the reception selector in a switching
manner, and

receiving the status signals from the transmission FIFO circuit and the
10 reception FIFO circuit, when the reception FIFO circuit is in a data writable
state and the transmission FIFO circuit is in a data unwritable state,
connecting the first selector with the transmission signal system and
connecting the second and the third selectors with the transmission selector in
a switching manner.

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